adam@whiteplain.com

Adam Doehling

Denver Metro Area, CO

Qualifications

RTL Design for FPGA and ASIC development

- Experience with development of custom Verilog RTL, including encryption, DDR controller, CPU, and others
- Comfortable with both FPGA and ASIC development practices, including Altera / Xilinx / Synopsys toolchains
- Knowledge of modern testbench design and UVM practices, capable performing simulation debug / analysis

Strong Circuit and PCB Design Skills

- Experience implementing many digital interfaces on a card level, e.g. PCIe, SATA, SAS, USB, DDR, LVDS, Ethernet
- Excellent debugging ability, comfortable in lab environment with many forms of test equipment, including rework
- Ability to perform channel, waveform, and timing simulation / analysis on a variety of parallel and serial interfaces
- Comfortable with EDA toolchains, including Cadence / Mentor design tools, Quantum SI, Hyperlynx
- High density board design / layout, including blind / buried vias on up to 20 layers
- Board and System Architecture, Specification, Test Plan development and execution
- Analog design, e.g. DC-DC buck/boost, ADC / DAC, Power Budgets, Design for EMC / EMI

Solid Software Background

- Board bringup and software configuration for multiple software platforms, including Linux on ARM and PowerPC
- Developed userspace and driver software in C/C++, Assembly, VB, and Java for product design and/or testing
- Crafted custom analysis and test programs for project needs using scripting languages (Perl, Python, Matlab)

Work History

WhitePlain Engineering - (Jan 2017 to Present) - Owner and Engineer - *Arvada, CO*

- Designed FPGA and PCB hardware, along with low level kernel driver modifications for networking applications
- Performed FPGA and DMA driver development for Windows for high speed video application
- Developed wireless protocol and hardware to support very low power sensor accessories for consumer devices

Oracle - (Aug 2012 to Jan 2017) - Hardware Design Engineer - *StorageTek* - *Broomfield, CO*

- Product development engineer working on Tape Drive digital design
- Developed RTL for encryption, processor, DDR memory, and other SoC components for high speed data transfer
- Worked with FPGA and ASIC vendors for both prototypes and final design deliveries
- Create testbenches and supported verification team on both RTL and gate level simulations
- Supported various card level design and analysis for the Tape Drive, including schematic and layout design / review

Plexus Engineering Solutions - (Jan 2008 to Aug 2012) - Digital Hardware Engineer - *Louisville, CO*

- Product development in Networking & Communications, Industrial & Commercial, Defense, Medical sectors
- Experienced in all aspects of product design, from concept, spec, design, prototyping, test, to manufacturing
- Consistently delivered on 10+ projects in multiple roles; e.g. System Lead, Digital Lead, and independent roles
- System lead on a COM-Express board design | Digital lead for a medical product utilizing an ARM / touchscreen
- Designer for high density board for the defense industry | PCIe HBA design for SAS and Fibre Channel cards
- Functional test design, transition and support for manufacturing on multiple programs
- Provided input to project proposals & quotes, supported multiple business development meetings & activities

University of Washington - (Sep 2006 to Dec 2007) - Teaching Assistant - *Seattle, WA*
Boeing Satellite Development Center - (Summer 2006, 2007) - Internships - *El Segundo, CA*
Micron Technology - (Summer 2005) - Internship - *Boise, ID*

Education

University of Washington - (Sep 2006 to Dec 2007) - *Seattle, WA*

Master of Science in Electrical Engineering, emphasis in Controls / Robotics, 3.75 GPA

University of Colorado - (Aug 2002 to May 2006) - *Boulder, CO*

Bachelor of Science in Electrical and Computer Engineering, Graduated Magna Cum Laude, 3.89 GPA